



TECHNOLOGY DEVELOPMENT PLAN FOR THE BASELINE DETECTOR SYSTEM OF THE X-RAY MICROCALORIMETER SPECTROMETER (XMS) OF THE INTERNATIONAL X-RAY OBSERVATORY (IXO)

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1 REVISION HISTORY

Revision	Date	Changes
–	June 13, 2010	Initial release

2 INTRODUCTION

2.1 Purpose

The primary purpose of this document is to present the technology development plan for the XMS detector system. It covers the current status (including assessment of the Technology Readiness Level, TRL, and a justification of the level assigned), the roadmap to progress to a level between TRL 5 and TRL 6 by the middle of 2012, and an assessment of the associated cost. A secondary purpose of this document is to address the Action Items raised at the XMS Phase-A Study Mid-Term Review that pertain to the detector system (AI #4, #8, and #9).

2.1.1 Relevant action items from Mid-Term Review and sections where addressed

{AI #4} – In terms of TRL, the scaling of 32x32 to 40x40 pixels for the core array shall be duly justified. *Section 5.3.2.1.*

{AI #8} – Provide evidence that the baseline GSFC array design can be improved in terms of thermal cross-talk. *Section 5.3.3*

{AI #9} – Background analysis: estimate number of events that will be absorbed in the Si frame and could cause ‘deadtime’ in the array. *Section 5.3.2.2.*

Search on {AI #N} to jump quickly to the sections where these points are addressed.

2.2 Scope

For the purpose of this document, the Detector System is defined as the composite science array (central array and outer array) combined with their multiplexed SQUID read out. The development plan advances the detector and read-out technologies separately and brings them together for integrated milestones. The development plans for the anti-coincidence detector and the focal-plane assembly (mechanical, electrical, and thermal staging of the detector and cold read-out components) are not addressed in this road map, although it is presumed that the TRL 6 demonstration incorporates both an anti-coincidence detector prototype and staging of the components in a manner approaching a flight-worthy design.

2.3 Overview of the Detector System Baseline

The reference design for the XMS detector system consists of a composite array of close-packed transition-edge sensor (TES) x-ray calorimeters read out by SQUID multiplexers. The baseline for the detector system design is based on the technical approach that is most mature today. Mo/Au transition-

edge sensor (TES) thermometers with Bi/Au thermalizing x-ray absorbers comprise the arrays. A 40 x 40 central array, arranged on a 0.3 mm (3 arc sec) pitch, is contained within a 52 x 52 array of 0.6 mm pixels. In the outer array, 4 pixels are read by a single TES, and discrimination between the four positions is achieved via pulse-shape analysis. The outer array contains 576 TES thermometers, compared with the 1600 of the inner array. In the baseline time-division multiplexing (TDM) concept, the outputs from the dedicated input SQUIDS of individual TES pixels are coupled to a single amplifier, and multiplexing is achieved by sequential switching of these input SQUIDS. The reference design is based on 32-row multiplexing, with which the entire XMS focal plane array could, in principle, be instrumented with 68 signal channels. In order to avoid mixing inner-array and outer-array signals in a single multiplexer channel, however, the baseline is 72 signal channels. Heat sinking of the frame of the arrays to the 50 mK stage is achieved via gold wire bonds to gold-coated areas on the array frame, into which heat from the underlying substrate is coupled. Heat sinking within the silicon grid of an array is achieved via incorporation of a metallic grid. Justification for this choice of baseline design, a discussion of the operating principles, and much more detail about the design and operation of the baseline detector and read-out technologies (and alternate approaches) can be found in the trade-study documents for the XMS detectors (GSFC-XMS-RP-2010-006) and the multiplexer (SRON-XMS-RP-2010-007).

3 REFERENCE DOCUMENTATION

GSFC-XMS-RP-2010-006 (SRON document library) – XMS Detector Trade Study

SRON-XMS-RP-2010-007 (SRON document library) – XMS Read-out Trade Study

SRON-XMS-PL-2010-025 (SRON document library) – Focal Plane Assembly Development Plan

IXO-TN-001141 (GSFC document library) – XMS Noise Budget

(Kilbourne-Doriese-SPIE2008) Kilbourne CA, Doriese WB, et al., 2008, “Multiplexed readout of uniform arrays of TES x-ray microcalorimeters suitable for Constellation-X”, Proc. SPIE, 7011, 701104.

TEC-SHS/5551/MG/ap (ESA) – TRL Handbook, Iss. 1, Rev. 6

4 TECHNOLOGY DEVELOPMENT STATUS

The integrated XMS detector system technologies reached Technology Readiness Level (TRL) 4 in March 2008 with the successful demonstration of multiplexed (2x8) read-out of 16 different pixels (in an 8x8 array) similar to what is needed for the current XMS reference design (Kilbourne-Doriese-SPIE2008). Reaching this milestone showed that the baseline technology approach for the XMS core array is fundamentally sound. The detector pixels were sufficiently uniform to permit good performance to be achieved under common bias, and the modest degradation of the detector performance while multiplexed was consistent with models. Resolution across 16 multiplexed pixels ranged from 2.6 eV to 3.1 eV, and the pulse time constant was 0.28 ms. Additionally, 12-channel and 16-channel multiplexing were accomplished with degraded resolution (average resolutions of 3.0 and 3.2 eV, respectively).

This “2x8 demo” achieved the most fundamental goal of a demonstration of TRL 4 (as articulated on pg. 3 on the ESA TRL Handbook, Iss. 1, Rev. 5) – basic technological components were integrated to

establish that they will work together. The performance approached the requirements of potential system applications (in terms of resolution, speed, pixel scale, and quantum efficiency.) However, consistent with the expectations for TRL 4, the validation was relatively low-fidelity compared with the eventual system application. It was low fidelity in that it is not possible to scale up the technologies used in the demonstration to what is needed for the flight system without further technology development. Some progress on the needed further development has been made since the TRL 4 milestone, which will be presented in the discussion of the technology development plan.

The baseline approach to the outer array, in which 4 pixels are read by a single TES (called a Hydra), has been demonstrated with 0.25 mm pixels. Resolution of 6 eV and position discrimination were achieved. More significantly, a robust model has been established that describes the device behavior, and when scaled to the pixel size of the baseline outer array, verifies the suitability of the approach for the XMS reference. (See GSFC-XMS-RP-2010-006.) The outer array has not had a multiplexed read-out demonstration on any array or pixel scale. In the development plan, the core array drives the read-out development, and it is assumed that the same read-out architecture can be used for the outer array pixels. This is a reasonable assumption because the pulses of the outer array are slower by about a factor of 6, but preserving the line rate and high-frequency roll-off of the core array channels for the outer array preserves the bandwidth needed to discriminate between the different pixels of a single Hydra by characterization of the pulse rise times. Since the read-out of the outer array is identical to that of the inner array, the fabrication processes and materials of the outer array are identical to the inner array, there has been a successful proof of principle of the Hydra concept, and a robust detector model has been developed, the TRL 4 designation extends to the entire detector system.

The designation of TRL 4 requires that the following four criteria be met – 1) that the technology concept and its required function be well-defined, 2) that the specific requirements placed on the technology by the prospective application be identified and defined, 3) that the ability of the technology to meet the requirements of the prospective application be verified through rigorous testing and modeling, and 4) that there be a viable path forward to the ultimate requirements of the application. The whole of this technology development document, in essence, is a defense of the TRL 4 designation, since it starts with a specific reference technology, discusses the characteristics demonstrated to date, discusses the characteristics that it needs to demonstrate to meet the XMS requirements, and presents the plan to do so. In the next paragraph, we summarize the case that we make in more detail in the rest of this document.

At the pixel level, the design is well in hand. A very specific pixel design, based directly on the successful arrays used for the 2x8 readout demonstrations, has been established as the reference design (see GSFC-XMS-RP-2010-006). The main challenge at the pixel level is presently process control, which is mainly a matter of allocating sufficient resources to tracking and controlling the superconducting transition temperature (T_c) of the Mo/Au TES and the heat capacity of the Au/Bi absorber. At the array level, there is a solid foundation for arrays at the 8x8 scale (including uniformity and thermal characterization), and there has been strong progress towards the 32x32 scale. Concepts for key components of a large array, high-density wiring and array-scale heat sinking, are well defined and are presently under development. The degree of heat sinking needed has been defined and determined to be feasible. The specific multiplexer architecture is based on the TDM used for the 2x8 readout demonstration, with well-defined specific changes implemented to increase the bandwidth, and thus improve and extend the performance of the demonstration to 32 rows. Close to the required bandwidth and noise performance has been demonstrated at the electronics level. A joint optimization study of the detectors with the readout (in which the free parameters were the bias resistance and the TES thermal conductance and the circuit inductance was chosen to achieve critical damping) revealed the parameter

space over which the XMS resolution and counting rate requirements could be met with realistic SQUID noise. This study took into account the effect of finite record length on the resolution (which was case dependent), and provided the shunt resistor and thermal conductance values used in the reference design (which ended up being similar to existing test set-ups and devices). In the end, the combined reference design of the detectors and read-out, in a configuration meeting the counting rate requirements, has a spectral resolution of 2.3 eV. The XMS noise budget (IXO-TN-001141) allocates the quadrature difference between that and 2.5 eV to various other systems and effects that have impact on the achievable resolution. Therefore, the technology concept is well defined; the derived requirements are understood; the capacity of the technology to meet the mission requirements has been verified; and there is a viable path forward to TRL5 and beyond.

5 TECHNOLOGY DEVELOPMENT PLAN

5.1 Approach and Organization

The XMS detector system technology development roadmap consists of major milestones tied to significant demonstrations of the integrated detectors and read-out electronics, each fed by supporting demonstrations in the detector and superconducting electronics components separately. Two of these major milestones bring the inner and outer arrays individually to TRL 5, another demonstrates that the inner and outer arrays can be run together, along with the anti-coincidence detector, at the fidelity of TRL 5, and the final milestone establishes TRL 6.

Each of the technologies supporting the XMS is at Research and Development Degree of Difficulty (R&D3) II, which means that there remains a significant amount of development work, but that the path to success is sufficiently straightforward that parallel development of significantly different alternate technologies will not be necessary. This approach is low risk as long as sufficient investment in the primary development path is made early in the program.

In the rest of this section, the major milestones are presented, each followed by a list of the supporting milestones associated with it, justification of the requirements stipulated for successful completion of the milestone, and discussion of the technical approach. Projected dates for each major and supporting milestone are included in brackets after the definition of each milestone. As would be expected, the dates of the supporting milestones generally precede the associated major milestone, but environmental testing needed to support the TRL claim of a major milestone, but not needed for the functional demonstration itself, may occur after the associated major milestone. Graphical representation of the schedule is shown on the final page.

5.2 Extended Field-of-View Concept Demonstration

5.2.1 Requirements for successful completion of the milestone

Verify the feasibility of 4-pixel Hydra devices with absorbers on a 0.6 mm pitch. This milestone requires demonstrating a resolution on each pixel of a Hydra device of better than 15 eV in a close-packed array. Design characteristics (T_c , quantum efficiency, thermal conductance values of all the thermal links), are not required to match the reference design precisely, but should be close enough to permit more certain extrapolation to the reference design than has been possible with the tests of smaller Hydras. [JULY 2010]

5.2.2 Discussion and justification of the milestone requirements

Although the resolution requirement for the outer array is 10 eV, performance better than 15 eV on all pixels of a Hydra is sufficient to meet this milestone if the performance can be explained by a quantitative model and the steps needed to improve the performance can be identified. The demonstration should verify position discrimination with the same pulse shaping needed for multiplexing. Although the allowed dead time per Hydra is a factor of 6 longer than for a pixel of the core array, using the same architecture for the multiplexed read-out preserves sensitivity to the variations in the pulse shape, and allows the outer array to be read with 18 electronics channels identical to the 50 used to read out the core array. Thus, the outer-array concept demonstration only needs to validate the detector technology and not its TDM read out, as long as the pulse shaping used in the test is consistent with the slew-rate limits of the TDM baseline design (SRON-XMS-RP-2010-007).

5.2.3 Technical approach to reaching the milestone

The Hydra design to be demonstrated has nearly 6 times the absorber area per TES as the proof-of-concept design that achieved 6 eV resolution. In order to meet the 10 eV resolution requirement in the scaled-up device, a lower operating temperature has been chosen (75 mK rather than 90 mK). A design has been devised and modeled based on absorbers that are 1 μm Au and 4 μm Bi with estimated total heat capacity of 10.8 pJ/K. The reduction in operating temperature comes at some penalty in temperature stability. However, since the baseline resolution is already 9.5 eV, a 1 eV noise term (estimated impact of the core-array temperature stability requirement on the outer array) has minimal impact. Applying all of the requirements of the core-array noise budget to the outer array, the average energy resolution across all 4 pixels of a Hydra is predicted to be about 11 eV (IXO-TN-001141). It is unlikely that this technology will be able to meet the outer array requirements with adequate margin in the noise budget, but alternative designs for the outer array would greatly increase the complexity of the design for the focal-plane assembly. Thus we will consider the Hydra approach to be a viable design for the outer array even if projected in-flight performance based on the measurements associated with this milestone does not quite reach 10 eV.

5.3 Core Array Prototype (TRL 5) Demonstration:

Demonstrate multiplexed (3 columns x 32 rows) read-out of 96 different flight-like pixels on a 0.3 mm pitch in a 32x32 (or greater) array with > 95% of pixels achieving better than 3-eV resolution at 6 keV, when analyzed using a record length and pre-pulse exclusion interval consistent with the requirement of 80% live time at an x-ray rate of 50/s/pixel. The 96 pixels used in this test must span the full range of positions in the array, with respect to distance from the edge of the array. Verification must also be accomplished at count rates up to the equivalent of 50 counts/s/pixel at 1 keV (see discussion below), in those pixels located in a valid test environment (either surrounded by other biased pixels or by unbiased pixels that are shielded from x-rays). [DECEMBER 2010]

5.3.1 Supporting milestones:

- 32-channel MUX switching speed and low noise demonstration [SEPTEMBER 2010]
- verification of 32x32 close-packed (flight-like, 0.3 mm pitch) array, in test of at least 16 randomly distributed pixels, each meeting XMS requirements for the core array when tested individually (or via a lower degree of multiplexing, e.g. 8 row). Verification must be accomplished at count rates up to 50 counts/s/pixel at 1 keV (see discussion below), in those pixels located in a valid test environment (either surrounded by other biased pixels or by unbiased pixels that are shielded from x-rays). Resolution for x-rays greater than 7 keV (e.g. using Ni K α fluorescence) should be determined in order to estimate the

resolution at 7 keV, the highest energy at which the 2.5 eV requirement is specified. [SEPTEMBER 2010]

- verification that minimum ionizing particles interacting with the frame of the calorimeter array will not cause an unacceptable dead time when scaled up to the full scale of the detector frame and the cosmic-ray rates expected at L2. [SEPTEMBER 2010]
- successful vibration testing of 32x32 array [DECEMBER 2010]

(Note that radiation testing is deferred and considered part of the integrated TRL 5 milestone, since radiation effects are not specific to the core array or outer array individually, and their read outs are identical.)

5.3.2 Discussion and justification of the milestone requirements

5.3.2.1 Overall requirements of the milestone demonstration

The statement of the resolution requirement ($> 95\%$ of pixels achieving better than 3-eV resolution at 6 keV) for this milestone is meant to accommodate a distribution of results around a mean near 2.5 eV. The specific instrument requirement for the uniformity is still under discussion, but proposed definitions are similar to the statement proposed for this milestone.

Vibration will be done at the component level. Since the detector system is not yet integrated in a flight-like assembly, the only vibration testing that is useful at this stage is of the pixels, to confirm that the membranes are robust.

This demonstration requires the SQUID multiplexer to be at the ultimate design speed (8 MHz open loop bandwidth), which will be realized with straightforward design changes from the successful 2x8 demonstration. {AI #4} The development required in scaling the core array from 8x8 to the present 40x40 baseline lies mainly in routing of the signal leads through the array (fine-line microstrips are now required) and in heat sinking the array structure to handle the bias power of 1600 pixels and minimize thermal crosstalk. These elements can be adequately verified in a 32x32 array, thus the milestone does not require the full 40x40 of the baseline. The microstrip technology is already in hand, and the process of integrating it into the TES array fabrication is in progress, but has already produced operable arrays. The width and spacing for the wiring in the 32x32 array that will be used in the TRL 5 demonstration is already sized at a scale appropriate for implementation on a 40x40 array. A 40x40 array will have 56% more pixels, and thus 56% more bias power that needs to be conducted to the heat sink, compared with a 32x32 demonstration array. The thermal characteristics of the demonstrated array must be extrapolated to the XMS core array, but an extrapolation by less than a factor of two can be done with a high degree of certainty. In the next section concerning the technical approach, the plans for improving the heat sinking, and the evidence that the approach will be sufficient in a 40x40 array, will be discussed in more detail. In the rest of the present section, the measurements needed to verify that the requirements are met are discussed.

5.3.2.2 Verification of the thermal design

There are three aspects to this demonstration that verify the thermal design. The first is the demonstration of simultaneous operation of pixels in locations from the center to the edge. The second is the demonstration of performance at the required 50/s/pixel photon rate, which would verify that noise from thermal crosstalk is not significant. The third is determination of dead time from cosmic rays interacting in the frame. Each of these demonstrations must be accompanied by sufficient characterization to extend the results to XMS.

The first test needs correction not only for the difference between a 32x32 array and a 40x40 array, but also for the fact that it will not be conducted in an apparatus that can read out (or bias) the full 32x32 array. Pixels that cannot be read out should be biased in series so that the temperature gradient that would result from biasing them as sensors can be approximated.

The second test, the measurement of thermal crosstalk, is less affected by the scale of the test than the measurement of temperature gradients, since crosstalk noise is dominated by nearest neighbors and by the heat flow away from the immediate vicinity of a pixel. In fact, care must be taken so that the crosstalk test of the demonstration array is not more severe than the actual flight case. Because electrothermal feedback reduces the magnitude of the pulse of heat that reaches the frame of an array when an x-ray is absorbed in a biased pixel, a pixel that is adjacent to pixels that are illuminated but not biased in their transitions will be subjected to more thermal crosstalk noise. Additionally, because thermal crosstalk noise scales as $Er^{0.5}$, where E is the energy and r is the count rate, a test at 50/s/pixel using 6 keV x-rays would not be a valid test, since the mean energy of a celestial x-ray spectrum is much less than 6 keV. In order to demonstrate that the thermal crosstalk noise from 50/s/pixel of 1 keV photons does not degrade the resolution, a test using 6 keV x-rays only needs good resolution up to a rate of 1.4/s/pixel, remarkably. (At that rate, a correction for shot noise in the sparse limit needs to be applied.) Characterization of the crosstalk directly (via record averaging) and by measurement of the resolution as a function of count rate is required for confident extrapolation to the flight system. Measurements over a range in energy as well as rates should be a goal, but not a requirement, for this milestone.

{AI #9} Energy deposited into the frame of the array results in a pulse of the effective heat-sink temperature, which causes signal pulses on all the pixels. In order to accommodate wire bonds contacts, a leading concept for the ultimate layout of the core array chip has approximate dimensions of 8 cm x 8 cm, with only the central 1.2 cm² area occupied by the 40x40 array. At a rate of 2/s/cm² for Galactic cosmic rays in a flat detector, and not even considering secondary particles, each pixel potentially could see a rate of well over 100/s without x-rays. Although such events would be flagged and rejected by coincidence between pixels, they would result in a minimum dead-time of ~50% if they are large enough to trigger. Therefore, it is a requirement to design the array such that only a few percent of minimum ionizing particles traversing the frame of the array result in pulses on the pixels. Scaling from models run for Suzaku/XRS, this stipulation requires that the peak of the minimum ionizing spectrum lie about a factor of 15 below the trigger level. The apparent energy of the coincident pulses relative to the energy of the impulse into the frame scales as the ratio of the thermal conductance of a pixel to the thermal conductance of the heat sinking, in cases for which the time constant for heat to leave the chip is faster than the electrothermal time constant of the pixels. For 200 pW/K and 10 μ W/K for the reference design pixel conductance and the chip heat sinking, respectively, we get that the 120 keV peak of the minimum ionizing spectrum in a 0.3 mm thick Si frame shows up as 2.4 eV pulses on the array. In such a case, with a trigger at 30 eV, the cosmic rays into the frame would result in ~1% dead time. The impact on the noise from the pulses that are not triggered needs to be properly assessed, but a quick estimate shows it could be significant (> 1 eV), and may need to be mitigated by adding sufficient heat capacity to the frame to shift the noise power to low frequencies.

In this milestone demonstration, a first assessment of the impact of cosmic rays in the frame of the array is made in a long acquisition in the absence of x-rays; coincidence between background events on multiple channels is a signature of energy deposited in an insufficiently heat sunk frame. Irradiating the frame with alpha particles allows direct measurement of the sensitivity to energy into the frame.

5.3.2.3 Justification of TRL 5 designation

This milestone is consistent with the requirements for TRL 5 because the full detector requirements will be demonstrated at the detector/read-out subsystem level, and scaling up requires adding more pixels, MUX chips, etc., but no new technology development. Thus it is a significantly higher-fidelity demonstration than the 2x8 array/MUX demonstration. Cryogenic detectors are operated in a relevant environment by definition; the laboratory cold platform will be sufficiently well characterized (in terms of temperature control, pick-up noise, microphonics, etc.) to understand its contribution to the detector noise budget so that extrapolation to the flight system noise budget can be done. Compelling arguments (from analysis and modeling) will connect the measured performance in specific test cases (such as resolution as a function of incident x-ray rate) to the needed performance in a flight-like configuration.

5.3.3 Technical approach to reaching the milestone

The baseline design presumes the same detector characteristics as the pixels of the 8x8 array used for the 2x8 demo, including the heat capacity, which is accomplished through using 1 μm Au and 4 μm Bi. This sort of composition has been used successfully in even larger pixel designs and is not expected to present any complications (although occasional incidents of significantly higher heat capacity in the Bi underline the need for investment in process control). The integration of microstrip wiring with the TES process has already gone through several refining iterations and no major change in approach is anticipated. Pixels in 32x32 arrays are already being characterized through microstrip leads, and, in a recent test, 12 out of 14 channels showed identical IV curves.

{AI #8} The needed improvements in heatsinking are understood and are achievable. The application of a Cu layer to the back of the array grid has already been demonstrated sufficient to handle the bias power of a full 40x40 array (via measurement of its conductance and calculation of the resulting thermal gradient expected in the XMS array). This metalized grid is not adequate for controlling thermal crosstalk, however, because the heat needs to spread out over several unit cells of the silicon grid before it can effectively couple into the metal on the back (due to electron-phonon coupling and boundary resistances). Coupling to that heat-sinking grid needs to be improved by a factor of 2-3 to maintain crosstalk noise below the level allocated in the noise budget. The short-term plan to achieve this is to remove processing residue from the sidewalls of the silicon frame that define the membrane area of each pixel and to coat those walls with heat-sinking Cu via angled evaporation. This increases the area for coupling into the Cu by a factor of 3. Metallization of the sidewalls of the wells under each membrane will soon be characterized. Top-side metallization, using planarized electroplated microtrenches capped by an insulator, atop which the microstrip leads are run, would allow for even stronger heat sinking. Such structures have been developed, but have not yet been integrated into array processing.

Heat sinking of alumina detector boards via gold wire bonds to thick gold-coated regions of the boards has achieved conductances at 50 mK at the required 10 $\mu\text{W/K}$ needed for the array as a whole, but similar heat sinking of detector chips thus far has not achieved better than about 1 $\mu\text{W/K}$, despite similar quantities and lengths of the wire bonds. An important difference may be the thickness of the gold (6 μm for the alumina boards, typically 1 μm for the detector heat sinks), thus the use of a thicker heat sinking layer on the detector frame, at least under the region of the wire-bond contacts, will be investigated.

In order to move from the 2x8 demo to TRL 5, the TDM switching speed needs to be increased by a factor of 4, from a line rate of 1.56 MHz to 6.25 MHz. This is achieved in a new architecture that has a two-times faster clock and two-times faster algorithm than the system used for the earlier demonstration. This faster switching needs a commensurate increase in bandwidth, which is to be accomplished by reducing the stray inductance in the wiring in each column between the second-stage

SQUID at 50 mK and the series array SQUID run at 1–4 K, by the replacing the series array with a low-power version that can be operated at 50 mK. The signal from the low-power series array is amplified by a broad-band, low-noise, flat-response pre-amplifier such as the commercially available Magnicon XXF pre-amplifier. Close to the necessary switching speeds (settling times) have been demonstrated in component tests, but need to be verified in the integrated system.

5.4 Outer Array Prototype (TRL 5) Demonstration

Demonstrate multiplexed (2 columns x 32 rows) read-out of 8x8 array of four-absorber Hydras (same physical area covered as 32x32 core array demo) with better than 15 eV resolution at 6 keV when analyzed using a record length and pre-pulse exclusion interval consistent with the requirement of 80% live time at an x-ray rate of 2/s/pixel, and position discrimination down to energies as low as 150 eV. [DECEMBER 2011]

5.4.1 Supporting milestones

- demonstration of pulse-shape discrimination and 32-channel multiplexing at compromise choice of input filtering [SEPTEMBER 2010]
- verification that 8x8 or greater array of close-packed, multi-absorber TES devices can be fabricated with sufficient uniformity for common biasing, meeting the requirements for the extended array on all pixels [JUNE 2011]
- successful vibration testing of outer-array prototype [DECEMBER 2010]

5.4.2 Discussion and justification of the milestone requirements

This milestone verifies that the Hydra concept can be implemented with sufficient uniformity and read out with the same basic TDM system as the core array. The performance requirement has been left at 15 eV to accommodate a distribution of results around a mean near 10 eV.

Verification of energy discrimination down to 150 eV may be accomplished with escape events and the electron-loss continuum in spectra with higher energy lines.

The thermal design of the Hydra array will be verified in a manner analogous to the tests planned for the core array demonstration.

The TRL 5 justifications cited for the core-array read-out demonstration apply equally to the outer-array read-out demonstration.

5.4.3 Technical approach to reaching the milestone

Most of the technology development needed for this milestone is accomplished in the prior milestones. The microstrip read-out and array heat sinking are developed for the TRL 5 demonstration of the core array, and the proof-of-concept for Hydras at the scale needed for the IXO XMS reference design develops most of the array details. There will be an optimization of the parameters between the fabrication of the proof-of-concept and TRL 5 Hydra demonstration arrays.

Optimization of the coupling of the Hydras with TDM will start with the Hydra proof-of-concept demonstration, and will involve signal models as well as proofs of concept.

5.5 Integrated Detector-System Prototype Demonstration (TRL 5)

Combine the requirements of the core-array and outer-array TRL 5 demonstrations into an integrated demonstration of both parts of the focal plane. An anti-coincidence detector will also be integrated into the test platform and operated. [DECEMBER 2012]

5.5.1 Supporting milestone

- test layout defined [JUNE 2012]
- successful radiation testing of SQUIDs and detectors [SEPTEMBER 2012]

5.5.2 Discussion and justification of the milestone requirements

This demonstration verifies that there are no fundamental interferences between operation of the two science arrays and the anti-coincidence detector. (The technology development plan for the anti-coincidence detector is discussed elsewhere.) It begins to develop the issues associated with staging the different elements that reside within the focal-plane assembly, but not at the fidelity of TRL 6.

Radiation testing needs to be performed in a portable cryogenic test platform so that irradiation can be done while the parts are cold, and their performance can be measured without warming up. For SQUID components, measuring noise and $V-\Phi$ curves at 4 K before and after irradiation would be adequate, but radiation testing of the detectors needs to be done in an ADR. These radiation tests have been scheduled well after the separate performance demonstrations because of anticipated funding constraints. The radiation tests will complete the TRL 5 milestones of both the inner and outer array. Deferring radiation testing is low risk because SQUIDs have already been spaceflight qualified for Gravity Probe B. The TES devices themselves do not contain sensitive junctions and are unlikely to be susceptible to permanent radiation damage. The test will also investigate whether magnetic flux motion occurs when superconducting regions (e.g. leads or ground planes) are locally driven normal, which, while not permanent damage, could impact how the detectors are operated.

5.5.3 Technical approach to reaching the milestone

This demonstration will make use of the test components used to verify TRL 5 for the two arrays and anti-coincidence detector individually. This test will not involve redesign or scaling up to the array size needed for flight. All of the development activity will pertain to the staging of the components and handling the simultaneous signals from the three kinds of devices.

5.6 Detector Assembly Prototype Demonstration (TRL 6)

Multiplexed (6x32) read-out of portion of full composite focal plane array – 128 different single-TES pixels in a 40x40 core array and 64 multi-absorber TES (256 0.6-mm pixels) of a full-sized outer array meeting the IXO XMS requirements. A particle-veto has been integrated into the test set-up. Electrical and thermal interconnects and staging are approaching a flight-worthy design, but a flight design is not fully realized. All pixels are biased though not read out, in order to validate the thermal design. [OCTOBER 2013]

5.6.1 Supporting milestones

- verification of 40x40 core array [SEPTEMBER 2012]
- verification of full-sized outer array [SEPTEMBER 2012]

- composite detector vibration tests passed (using detector fixturing approximating that needed in focal plane assembly) [JANUARY 2013]
- electrical/thermal/mechanical assembly designed and fabricated [MAY 2013]

5.6.2 Discussion and justification of the milestone requirements

The difference between this demonstration and the Engineering Unit is that only the focal plane array will be of a flight-like design. The detector assembly will not be designed to accommodate every electronics channel, nor will it be engineered to vibration or mass specifications. The purpose of this demonstration is to bring the various components of the focal plane assembly together on the right scale to develop the technologies needed for their thermal and electrical integration into the focal plane assembly. The design of this assembly includes mechanical suspension systems, wiring interconnects, high-density wiring feedthroughs, thermal sinks, and kinematic mounts. The assembly must maintain the following at an acceptable level: 1) thermal stability, thermal gradient across array, and thermal crosstalk, 2) electrical crosstalk, microphonics, magnetic shielding, and susceptibility to interference, and 3) conducted and radiative heat loads on all the temperatures stages. The design of this assembly will be guided by experience with Suzaku/XRS, the X-ray Quantum Calorimeter and Micro-X sounding rocket programs, and laboratory test platforms. The design does not require new physics, but will require systematic quantification of materials parameters and a careful balancing of the competing needs of the electrical, thermal, and mechanical elements of the integration. The risks associated with this development can be minimized by allocation of adequate resources to this development.

5.6.3 Technical approach to reaching the milestone

Aside from actually producing arrays of the full scale, all the technology development leading to TRL 6 is concerned with the packaging of the detector and MUX components into the focal-plane assembly. While it is not the purpose of this demonstration to build a flight-like assembly, it will verify some of its essential elements. Engineering development will continue for the TDM components although the technology will be at the required performance level at the successful attainment of TRL 5. This engineering development includes optimizing the form-factor of the MUX chips for the XMS focal-plane layout, improving the yield of the SQUID components (from the present 25% yield), and refining the room temperature pre-amplifier.

6 BUDGET NEEDED TO SUPPORT THIS SCHEDULE

The assumption that funding until FY 2012 is limited to technology development funding pulled together or leveraged from various sources results in a very intense effort in FY12 and 13 to construct the TRL 6 testing infrastructure, design and carry out the radiation tests, and produce full sized arrays.

FY10: 2 M\$

FY11: 2 M\$

FY12: 4.5 M\$

FY13: 4.5 M\$

7 SCHEDULE GRAPHIC

